

ANDREW LOVELESS

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RESEARCH INTERESTS

My research interests are in developing new techniques to make embedded systems more fault-tolerant and resilient to attacks, as well as to reduce the performance overhead of fault tolerance approaches already used in embedded systems today. My work spans multiple areas, including distributed systems, real-time systems, networking, and security.

EDUCATION

University of Michigan Ann Arbor, MI
Ph.D. in Computer Science and Engineering Sep. 2018 – May 2023 (expected)
Advisors: Prof. Ronald Dreslinski and Prof. Baris Kasikci

University of Michigan Ann Arbor, MI
M.S. in Computer Science and Engineering Sep. 2018 – May 2021

Purdue University West Lafayette, IN
B.S. in Electrical Engineering Aug. 2008 – Dec. 2013

FELLOWSHIPS AND SCHOLARSHIPS

- National Science Foundation Graduate Student Research Fellowship Sep. 2020 – Present
Three year fellowship awarded to early-career Ph.D. students
- NASA JSC Engineering Directorate Academic Fellowship Sep. 2018 – Present
Allows me to continue working for NASA part-time while in graduate school
- Purdue Trustees Merit Scholarship Aug. 2008 – May 2013

AWARDS AND HONORS

- NASA Honor Award, Exceptional Technology Achievement Medal Aug. 2020
For the development and maturation of a fault-tolerant voting architecture using Time-Triggered Ethernet, leading towards adoption by the Gateway Program
- NASA Honor Award, Early Career Achievement Medal Aug. 2018
For outstanding and exemplary efforts in developing solutions for next-generation avionics networks and fault-tolerant computing
- [Nomination] NASA Advanced Exploration Systems Innovation Award Mar. 2018
For development of a fault-tolerant Time-Triggered Ethernet voting architecture
- [Nomination] Rotary National Stellar Team Award for Space Achievement Jan. 2018
Advanced Exploration Systems, Avionics and Software Team
- [Nomination] NASA Honor Award, Group Achievement Dec. 2017
Advanced Exploration Systems, Autonomous Systems and Operations Team
- NASA AES Certificate of Achievement Oct. 2016
Avionics and Software Team, FY16 Integrated Test
- NASA JSC Avionic Systems Division Recognition Award Oct. 2015
For development and maturation of the Time-Triggered Ethernet technology

PUBLICATIONS

- [1] Gatekeeper: A Reliable Reconfiguration Protocol for Real-Time Ethernet Systems. Brendan Luksik, **Andrew Loveless**, and Alan George. *IEEE Digital Avionics Systems Conference (DASC)*. San Antonio, TX, October 2021.
- [2] IGOR: Accelerating Byzantine Fault Tolerance for Real-Time Systems with Eager Execution. **Andrew Loveless**, Ronald Dreslinski, Baris Kasikci, and Linh Thi Xuan Phan. *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*. Nashville, TN, May 2021.
- [3] Optimal and Error-Free Multi-Valued Byzantine Consensus Through Parallel Execution. **Andrew Loveless**, Ronald Dreslinski, and Baris Kasikci. *IACR Cryptology ePrint Archive*. Online Manuscript, May 2021.
- [4] Development and Testing of a Vehicle Management System for Autonomous Spacecraft Habitat Operations. Gordon Aaseng, Jeremy Frank, Michael Iatauro, Christopher Knight, Richard Levinson, John Ossenfort, Michael Scott, Adam Sweet, Jeffrey Csank, James Soeder, Daniel Carrejo, **Andrew Loveless**, Tam Ngo, and Zachary Greenwood. *AIAA SPACE and Astronautics Forum and Exposition*. Orlando, FL, Sep. 2018.
- [5] A Proposed Byzantine Fault-Tolerant Voting Architecture using Time-Triggered Ethernet. **Andrew Loveless**, Christian Fidi, and Stefan Wernitznigg. *SAE AeroTech Congress and Exhibition*. Fort Worth, Texas, Sep. 2018.
- [6] A Modular, Scalable Avionics Architecture for Future Exploration Missions. Christian Fidi and **Andrew Loveless**. *AIAA SPACE and Astronautics Forum and Exposition*. Orlando, FL, Sep. 2017.
- [7] Approach for Sizing and Turndown Analysis of a Variable Geometry Spacecraft Radiator. Lisa Erickson and **Andrew Loveless**. *NESC Thermal and Fluids Analysis Workshop (TFAWS)*. Huntsville, AL, Aug. 2017.
- [8] On TTEthernet for Integrated Fault-Tolerant Spacecraft Networks. **Andrew Loveless**. *AIAA SPACE Conference and Exposition*. Pasadena, CA, Sep. 2015.
- [9] On Augmented DVH Analysis. **Andrew Loveless**, Arkajyoti Roy, Indra Das, and Omid Nohadani. *AAPM Annual Meeting and Exhibition*. Indianapolis, IN, Aug. 2013.

PRESENTATIONS

- [1] On Time-Triggered Ethernet in NASA's Lunar Gateway. *Avionics Architectures Community of Practice*. Online Talk, July 2020.
- [2] Building Compositional Systems with Time-Triggered Ethernet. *ESA TTE/cFS/IMA Workshop*. European Space Research and Technology Centre, Noordwijk, Netherlands, July 2018.
- [3] Using Time-Triggered Ethernet in the Core Flight System. *ESA TTE/cFS/IMA Workshop*. European Space Research and Technology Centre, Noordwijk, Netherlands, July 2018.
- [4] Mapping of SOIS Layering Concept to TTE/cFS. *CCSDS Fall Technical Meetings*. The Hague, Netherlands, Nov. 2017.
- [5] TTEthernet Development and cFS Integration. *Deep Space Gateway Open Software Multi-lateral TIM*. NASA JSC, Houston, TX, Sep. 2017.
- [6] Overview of TTE/cFS Integration. *CCSDS Spring Technical Meetings*. Southwest Research Institute, San Antonio, TX, May 2017.
- [7] Notional 1FT Voting Architecture with Time-Triggered Ethernet. *Avionics and Software FY17 Planning Meeting*. NASA JSC, Houston, TX, Nov. 2016.
- [8] Overview of TTE Applications and Development at NASA/JSC. *Invited Talk*. TTTech Computertechnik AG, Vienna, Austria, Oct. 2016.
- [9] Overview of TTE Applications and Development at NASA/JSC. *CCSDS Fall Technical Meetings*. ASI, Rome, Italy, Oct. 2016.

NASA NEW TECHNOLOGY REPORTS

- [1] MSC-26840-1: Core Flight Software Time-Triggered Ethernet Manager
- [2] MSC-26839-1: Core Flight Software Time-Triggered Ethernet Library
- [3] MSC-26370-1: Time-Triggered Ethernet Application for NASA's Core Flight System (cFS)
- [4] MSC-26369-1: Time-Triggered Scheduler Application for NASA's Core Flight System (cFS)
- [5] MSC-26364-1: Method for Ensuring Data Consistency Between Devices Using Time-Triggered Ethernet
- [6] MSC-26058-1: Software Library Extension for the TTEthernet Phoenix Intellectual Property

PROFESSIONAL EXPERIENCE

- **NASA Johnson Space Center** *Houston, TX*
Command and Data Handling Branch (EV2) Sep. 2018 – Present
Time-Triggered Ethernet (TTE) and Fault Tolerance Subject Matter Expert
 - Provide technical expertise on TTE and avionics fault tolerance techniques to the Gateway Program, as well as to international partners and commercial module providers.
 - Lead the technical direction of the Artemis Network Validation and Integration Lab (ANVIL), which is responsible for maturing the TTE technology for use in the Gateway Program.
 - Developed a novel and provably correct method for updating the network configurations of TTE devices in an active network, while minimizing disruption of existing traffic flows. *Work done in collaboration with the University of Pittsburgh.*
- **NASA Johnson Space Center** *Houston, TX*
Command and Data Handling Branch (EV2) Oct. 2016 – Aug. 2018
Avionics and Software (A&S) Project Command and Data Handling Lead
 - Led the development of a Time-Triggered Ethernet (TTE) based voting system that reduces size, weight, and power by eliminating the need for a fourth computer to tolerate a Byzantine fault. The system was successfully demonstrated in the Integrated Power, Avionics, and Software facility.
 - Wrote and maintained the TTE drivers and time-triggered scheduler for the Core Flight System, an open software framework used for a variety of spaceflight missions.
 - Successfully integrated 80+ data flows and 15+ applications from the A&S, Autonomous Systems and Operations, and AES Modular Power Systems projects for the A&S FY17 Integrated Test.
 - Helped update the Subnetwork Packet Service book for compatibility with time-triggered networks as part of the Consultative Committee for Space Data Systems (CCSDS) Spacecraft Onboard Interface Services (SOIS) working group.
- **NASA Johnson Space Center** *Houston, TX*
Command and Data Handling Branch (EV2) Mar. 2014 – Sep. 2016
Avionics and Networking Development Engineer
 - Built network drivers for several embedded platforms (e.g. Aitech SP0-100, Space Micro Proton 400K) and operating systems (e.g. RTLinux, VxWorks), forming the foundation for all future Engineering Directorate projects using TTE.
 - Extended the TTE technology by creating a full software-based IP network stack, increasing the max message size from 1500 to 64K bytes with <10% overhead, and enabling a demo of the Orion Ascent Abort-2 flight software during the A&S FY15 Mid-Year Integrated Test.
 - Identified eight pathstones enabling manned Mars exploration and presented suggested next steps and partnership opportunities to Engineering Directorate management as the networking domain lead for JSC's L-8 effort.

INTERNSHIPS

- **NASA Johnson Space Center** *Houston, TX*
Command and Data Handling Branch (EV2) Summer 2013

- Developed a network analyzer enabling the real-time visualization of hand controller commands sent from the Flight Deck of the Future to flight computers running in the Integrated Power, Avionics, and Software facility.
- **NASA Johnson Space Center** *Houston, TX*
Command and Data Handling Branch (EV2) Summer 2012
 - Developed a data acquisition system with custom I/O board and MCF51JF microcontroller that enabled the real-time monitoring and logging of pressure data from cold gas thrusters in the Integrated Power, Avionics, and Software facility.
- **NASA Johnson Space Center** *Houston, TX*
Spacecraft Software Engineering Branch (ER6) Spring 2011
 - Collaborated with Tietronix Software to design graphical user interfaces enabling crew of the Habitat Demonstration Unit to control camera and power subsystems from a portable tablet.
- **NASA Johnson Space Center** *Houston, TX*
Onboard Computer and Information Systems Branch (DS26) Summer 2010
 - Led knowledge capture program to archive technical specifications and other valuable records related to the Space Shuttle's avionic systems prior to retirement of the vehicle.
- **NASA Johnson Space Center** *Houston, TX*
Data Processing Systems Branch (DS22) Fall 2009
 - Completed core data processing systems flight controller training and Single Systems Trainer exams, and monitored Space Shuttle avionics in the Mission Control Center during STS-128 and STS-129.

UNDERGRADUATE RESEARCH

- **Purdue University** *West Lafayette, IN*
Fiber-Optic Controller for fMRI Testing (PI: Prof. Thomas Talavage) Fall 2013
 - Led a team of undergraduates designing a fiber-optic joystick for clinicians to use to evaluate a patient's higher cognitive function during functional magnetic resonance imaging (fMRI) tests.
- **Purdue University** *West Lafayette, IN*
Optimization in Radiation Therapy (PI: Prof. Omid Nohadani) Fall 2012 – Spring 2013
 - Created software enabling the quantitative comparison of radiation treatment plans based on historical data, allowing clinicians to distinguish plans that appear visually similar.
- **Purdue University** *West Lafayette, IN*
Electric Field Fringe Effect Simulation (PI: Prof. Daniel Elliott) Fall 2012
 - Developed models of electric field uniformity between conductor plates and produced results used in creating a new technique for measuring the amplitude of optical transitions in atomic Cesium.
- **Rice University** *Houston, TX*
Microscope Image Comparison (PI: Prof. Weiwei Zhong) Summer 2011
 - Developed algorithm to compare the clarity of photos taken by a microscope imaging robot in real time, reducing the number of pictures requiring manual review from 5K+ to <500 per run.

TEACHING AND MENTORSHIP

- **NASA Johnson Space Center** *Houston, TX*
High School Aerospace Scholars, NASA Mentor Summer 2020
 - Led a team of high school students planning a spaceflight mission over a week-long workshop.
- **University of Michigan** *Ann Arbor, MI*
Engineering Student Government Mentorship Program, Graduate Mentor Fall 2019 – Spring 2020
 - Met with undergraduate and graduate students to give advice on managing classes, performing research, and applying to Ph.D. programs.

- **Purdue University**

ECE 362: Microprocessor Design and Interfacing, Teaching Assistant

West Lafayette, IN

Spring 2012

- Administered two laboratory sections of a junior-level microprocessor design class, including giving lectures at the start of class, grading assignments, and assisting students in office hours.